Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claims 7, 10, 18 and 31, and amend claims 1, 8, 9, 11 and 21 as follows:

Listing of Claims:

1. (Currently Amended) A memory device, comprising:

a row address circuit operable to receive and decode row address signals applied to external address terminals of the memory device;

a column address circuit operable to receive and decode column address signals applied to the external address terminals;

a plurality of banks of memory cells arranged in rows and columns, each of the memory cells being operable to store a data bit written to or read from the banks at a location determined by the decoded row address signals and the decoded column address signals, a first one of the banks of memory cells containing a number of memory cells that differs from the number of memory cells contained in a second bank of memory cells;

a data path circuit operable to couple data signals corresponding to the data bits between the banks of memory cells and external data terminals of the memory device; ~~and~~

a command decoder operable to decode a plurality of command signals applied to respective external command terminals of the memory device, the command decoder being operable to generate control signals corresponding to the decoded command signals;

bank control logic that is operable to select the bank to which data are to be written or from which data are to be read; and

a mode register that may be programmed to select the length of data bursts when the memory device is operating in a burst mode, the bank control logic being coupled to the mode register to select the bank to which data are to be written or from which data are to be read based on the length of data burst programmed in the mode register.

2. (Original) The memory device of claim 1 wherein the first bank of memory cells contains a number of columns of memory cells that differs from the number of columns of memory cells in the second bank of memory cells.

3. (Original) The memory device of claim 2 wherein the first bank of memory cells contains a number of rows of memory cells that differs from the number of rows of memory cells in the second bank of memory cells.

4. (Original) The memory device of claim 1, further comprising a set of sense amplifiers for each of the banks of memory cells, the number of sense amplifiers in each set corresponding to the number of columns of memory cells in each of the banks.

5. (Original) The memory device of claim 1 wherein the memory device comprises a dynamic random access memory device.

6. (Original) The memory device of claim 5 wherein the dynamic random access memory device comprises a synchronous dynamic random access memory device.

7. (Cancelled)

8. (Currently Amended) The memory device of claim ~~8~~1 wherein the bank control logic that is operable to select the bank to which data are to be written to or read from based on the nature of the data.

9. (Currently Amended) The memory device of claim ~~8~~1 wherein the bank control logic that is operable to select the bank to which data are to be written to or read from is based on the source or destination of the data.

10. (Cancelled)

11. (Currently Amended) A memory subsystem, comprising:

a memory device, comprising:

a row address circuit operable to receive and decode row address signals applied to external address terminals of the memory device;

a column address circuit operable to receive and decode column address signals applied to the external address terminals;

a plurality of banks of memory cells arranged in rows and columns, each of the memory cells being operable to store a data bit written to or read from the banks at a location determined by the decoded row address signals and the decoded column address signals, a first one of the banks of memory cells containing a number of memory cells that differs from the number of memory cells contained in a second bank of memory cells;

a data path circuit operable to couple data signals corresponding to the data bits between the banks of memory cells and external data terminals of the memory device; ~~and~~

a command decoder operable to decode a plurality of command signals applied to respective external command terminals of the memory device, the command decoder being operable to generate control signals corresponding to the decoded command signals; and

a mode register that may be programmed to select the length of data bursts when the memory device is operating in a burst mode, the memory device being operable to select the bank to which data are to be written or from which data are to be read based on the length of data burst programmed in the mode register; and

a system controller having an address bus coupled to the external address terminals of the memory device, and a control bus coupled to external command terminals of the memory device, the system controller being operable to cause data to be written to and read from the memory device.

12. (Original) The memory subsystem of claim 11 wherein the system controller is operable to issue a bank address to the memory device to select the bank to which data are to be written or from which data are to be read.

13. (Original) The memory subsystem of claim 12 wherein the bank address issued by the system controller is based on the nature of the data written to or read from the memory device.

14. (Original) The memory subsystem of claim 12 wherein the bank address issued by the system controller is based on the source or destination of the data written to or read from the memory device.

15. (Original) The memory subsystem of claim 11 wherein the first bank of memory cells contains a number of columns of memory cells that differs from the number of columns of memory cells in the second bank of memory cells.

16. (Original) The memory subsystem of claim 15 wherein the first bank of memory cells contains a number of rows of memory cells that differs from the number of rows of memory cells in the second bank of memory cells.

17. (Original) The memory subsystem of claim 11, further comprising a set of sense amplifiers for each of the banks of memory cells, the number of sense amplifiers in each set corresponding to the number of columns of memory cells in each of the banks.

18. (Cancelled)

19. (Original) The memory subsystem of claim 11 wherein the memory device comprises a dynamic random access memory device.

20. (Original) The memory subsystem of claim 19 wherein the dynamic random access memory device comprises a synchronous dynamic random access memory device.

21. (Currently Amended) A computer system, comprising:

a processor having a processor bus;

an input device coupled to the processor through the processor bus to allow data to be entered into the computer system;

an output device coupled to the processor through the processor bus to allow data to be output from the computer system;

a data storage device coupled to the processor through the processor bus to allow data to be read from a mass storage device;

a system controller coupled to the processor through the processor bus, the system controller having an address bus and a control bus; and

a memory device coupled to the system controller, the memory device having an address bus and a control bus, the memory device comprising:

a row address circuit operable to receive and decode row address signals coupled to the address bus of the memory device from the address bus of the system controller;

a column address circuit operable to receive and decode column address signals coupled to the address bus of the memory device;

a plurality of banks of memory cells arranged in rows and columns, each of the memory cells being operable to store a data bit written to or read from the banks at a location determined by the decoded row address signals and the decoded column address signals, a first one of the banks of memory cells containing a number of memory cells that differs from the number of memory cells contained in a second bank of memory cells;

a data path circuit operable to couple data signals corresponding to the data bits between the banks of memory cells and external data terminals of the memory device; ~~and~~

a command decoder operable to decode a plurality of command signals applied to respective external command terminals of the memory device, the command decoder being operable to generate control signals corresponding to the decoded command signals; and

a mode register that may be programmed to select the length of data bursts when the memory device is operating in a burst mode, the memory device being operable to select the bank to which data are to be written or from which data are to be read based on the length of data burst programmed in the mode register.

22. (Original) The computer system of claim 21 wherein the system controller is operable to issue a bank address to the memory device to select the bank to which data are to be written or from which data are to be read.

23. (Original) The computer system of claim 22 wherein the bank address issued by the system controller is based on the nature of the data written to or read from the memory device.

24. (Original) The computer system of claim 23 wherein the bank address issued by the system controller is based on the source or destination of the data written to or read from the memory device.

25. (Original) The computer system of claim 21 wherein the first bank of memory cells contains a number of columns of memory cells that differs from the number of columns of memory cells in the second bank of memory cells.

26. (Original) The computer system of claim 25 wherein the first bank of memory cells contains a number of rows of memory cells that differs from the number of rows of memory cells in the second bank of memory cells.

27. (Original) The computer system of claim 21, further comprising a set of sense amplifiers for each of the banks of memory cells, the number of sense amplifiers in each set corresponding to the number of columns of memory cells in each of the banks.

28. (Original) The computer system of claim 21 wherein the memory device comprises a dynamic random access memory device.

29. (Original) The computer system of claim 28 wherein the dynamic random access memory device comprises a synchronous dynamic random access memory device.

30. (Original) The computer system of claim 28 wherein the processor is structured to execute an operating system, the operating system generating bank address and coupling the bank address to the memory device to determine the bank of memory cells to which data are written or from which data are read.

31. (Cancelled)

Claims 32-45 (Canceled)